Modeling and Measurement of Microstrip Transmission-Line Structures

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Abstract—New techniques have been employed in both the modeling and measurement of microstrip transmission-line structures. The modeling employs a dual potential approach using finite-element analysis to derive exact bounds to the microstrip characteristics. From these, error limits to the theoretical S-parameters of step-impedance-line structures have been derived.

The measurement of the S-parameters were performed on an automatic vector network analyzer using an "on-chip" calibration method with microstrip calibration pieces.

Theoretical results are presented for the test structures on both alumina and gallium arsenide, and measured results are presented for the alumina structure. Error bounds for the measured results have been derived from repeatability, and agreement between theoretical and measured results is reasonably good.

I. Introduction

THE USE OF microstrip transmission lines in the manufacture of microwave integrated circuits is widespread, and with the growing interest in gallium arsenide (GaAs) monolithic circuits, the need for accurate modeling of microstrip transmission-line structures is being reemphasized. Over the last 20 years, there has been a wealth of literature on the analysis and measurement of these structures, and an extensive list of references can be found in [1]. However, in past work, attention has rarely been paid to the estimation of the accuracy of the results. In this work, we attempt to put error limits on both the theoretical analysis and also on the measured results. By using a dual potential approach to the analysis of the microstrip structure, upper and lower bounds to the transmission-line parameters can be derived, from which the error limits of the S-parameters of a particular structure can be found.

The complex nature of the automatic network analyzer measurement equipment, and its calibration procedure, make the task of error estimation virtually impossible, and no attempt of this has been seen in the literature. The error bounds for the measurements are, therefore, derived purely from repeatability data gained experimentally.

II. Theory

The modeling of the microstrip transmission-line structures has been based on a dual potential finite-element (FE) analysis to derive exact upper and lower bounds to the solution. The finite-element approach was adopted due to its flexibility when applied to structures where there are large differences in the dimensions of the elements which comprise the structure. In microstrip, the inner dimensions may be two orders of magnitude smaller than the bounding dimensions. Now, given a transmission line with metallic conductors (electric walls) and lines of symmetry (magnetic walls), the potential satisfies Laplace's equation within the bounded cross section.

It is well known that a variational expression exists for the line capacitance of a uniform transmission line with applied potential V

$$\frac{CV^2}{\epsilon_0} = \int_S \int \kappa |\nabla \phi|^2 \, dS \tag{1}$$

where ϕ is the potential function within the cross section and κ is the local dielectric permittivity. Discretization of the potential over an aggregate of finite elements leads to a simple matrix equation [2] whose unknown is a column vector of discrete potential values.

Once the potential distribution has been solved using FE techniques, the line capacitance per unit length can be derived. However, by the minimum energy principle, only the exact potential distribution will result in the exact value for the capacitance, i.e., the FE solution is always an upper bound to the correct value. By interchanging the electric and magnetic walls, we derive the dual structure, and we can again solve the Laplace equation for the dual potential distribution. It has been shown [3] that this leads to a lower bound for the line capacitance. By solving the microstrip structure with and without the dielectric present, for both the dual potential distributions, exact bounds for both the characteristic impedance and the effective dielectric constant of the microstrip line structure can be derived from the following relations:

$$\epsilon_{\text{eff}} = C/C_0 \tag{2}$$

$$Z_0 = \sqrt{\epsilon_{\text{eff}}}/cC \tag{3}$$

where ϵ_{eff} is the effective dielectric constant, C_0 is the line capacitance without the substrate dielectric, C is the capacitance with the substrate dielectric, Z_0 is the characteristic impedance of the line, and c is the velocity of light *in vacuo*.

The important point to note here is that the exact solution must lie between these upper and lower bounds, and that these bounds may be brought closer together by implementing a finer mesh with more elements in the FE

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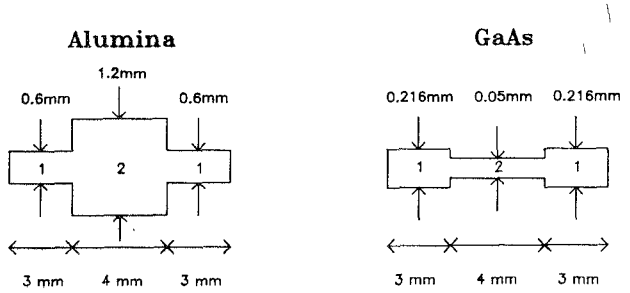


	Upper	Lower			Upper	Lower
Impedance (Ohms)	50.46	48.57	①	Impedance (Ohms)	50.73	49.22
Eff. Dielect. Const.	6.53	6.49		Eff. Dielect. Const.	8.26	8.19
Impedance (Ohms)	34.33	33.41	②	Impedance (Ohms)	83.88	79.82
Eff. Dielect. Const.	6.95	6.93		Eff. Dielect. Const.	7.58	7.55

Fig. 1. Step impedance line test structure layout.

analysis. So the accuracy of the solution is limited only by the power and memory capacity of the machine employed to do the computation. The absolute magnitude of the error in line capacitance itself is, therefore, known and the average of the bounds can realistically be assumed to provide an order of magnitude improvement in the accuracy.

The test structures examined in this work were step-impedance lines where there is a change in the width of the microstrip line. The dimensions of the lines on both alumina and GaAs are shown in Fig. 1. The upper and lower bound results are given in the table below the figure. From these, the bounds of S-parameters were derived by varying the impedance and effective dielectric constant values within their bounds. The chain matrix for each of the three line sections is given by

$$\begin{bmatrix} \cos(\beta 1) & jZ_0 \sin(\beta 1) \\ jY_0 \sin(\beta 1) & \cos(\beta 1) \end{bmatrix}$$

where Z_0 is the calculated characteristic impedance, $Y_0 = 1/Z_0$, and $\beta 1$ is the electrical length of the line (dependent on frequency and the calculated effective dielectric constant). The three chain matrices are cascaded into an overall chain matrix, which is then converted into the S-parameters of the line structure. This structure is symmetrical, i.e., $S_{11} = S_{22}$ and $S_{21} = S_{12}$, so only the S_{11} and S_{21} results are quoted here. This process is repeated many times to build up a range of possible S-parameters.

III. Measurement

Considering now the measurement technique, the S-parameter measurements were performed using standard automatic network analyzer equipment. However, the critical aspect of S-parameter measurement is the calibration routine to apply accuracy enhancement by error correction techniques [4]. If this is done using standard coaxial calibration pieces, then further processing of the results is required to remove the effect of the launcher which connects the coaxial test ports to the microstrip structure under test. This requires very accurate modeling of the launcher characteristics which is difficult particularly over broad frequency ranges. To try to overcome this problem, the approach of "on-chip" calibration is being considered by many workers. In this technique, the calibration pieces are formed in the same medium as the circuit under test, and the reference plane of the measurement on the circuit rather than outside it. A successful technique has been developed using coplanar waveguide calibration pieces [5], but for this work we have developed a technique using microstrip calibration pieces, because we wish to measure microstrip components. The calibration pieces used are a zero-length short circuit, open circuits at the ends of lines of known length, and a through line of characteristic impedance of 50 Ω. Software has been developed for standard 8- and 12-term error correction, and a series of measurement jigs built to accommodate test substrates of different substrate thicknesses. Measurements have been performed on substrates of both RT-Duroid and alumina.

Fig. 2 shows both the modeled and measured results for the alumina step impedance line, including both S_{11} and S_{21} magnitude and phase. The results are shown in terms of error bars, the two bars being slightly offset from one another for clarity. The error bar for the modeled results is derived directly from the upper and lower bound results of characteristic impedance and effective dielectric constant. For the measured results, it is extremely difficult to derive correct error bars due to the complex nature of the measurement equipment and the calibration process. The error bars shown are derived from statistical data of the repeat ability of several calibration and measurement operations. They are, therefore, likely to provide optimistic limits.

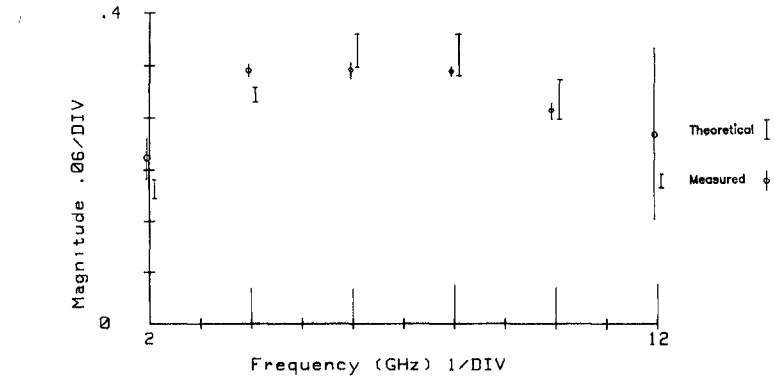
Fig. 3 shows the modeled results for the GaAs step-impedance line, again showing the range of predicted values.

IV. Contour Plots

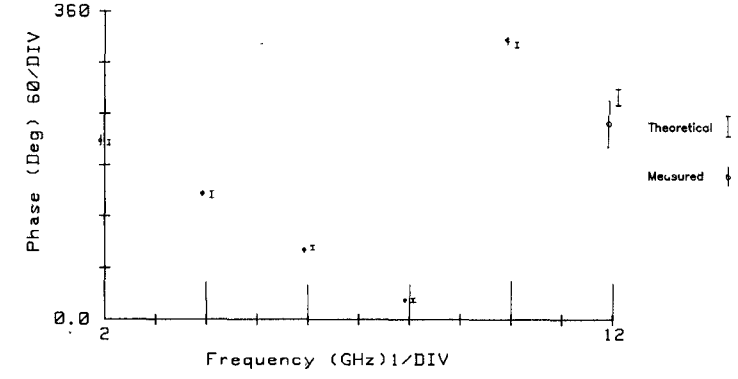
Since the introduction of the finite-element method, the solution to static field problems has provided an upper bound to the large scale parameters of the field (in our case, the capacitance per unit length—see (1)). Following earlier work [3] on the development of the theory of dual potentials, whose use results in a lower bound for the same large-scale parameters, finite-element techniques have been introduced [6] and applied to a variety of transmission-line structures including coaxial lines, stripline, and microstrip.

It has also been established [7] that the potential contours for the field problem and its dual are orthogonal as long as the medium remains piecewise continuous. This implies that, as a by-product of the solution of the finite-element matrix equation for upper and lower bounds to the capacitance per unit length, one also obtains a grid of dual potential functions orthogonal to each other — in other words, a contour of equipotentials for the problem in question and also the associated electric field contours.

Typical field contour plots are presented in pairs for one half cross section of a microstrip line in Figs. 4–7. Each pair shows contours for equipotentials in the original struc-



(a)



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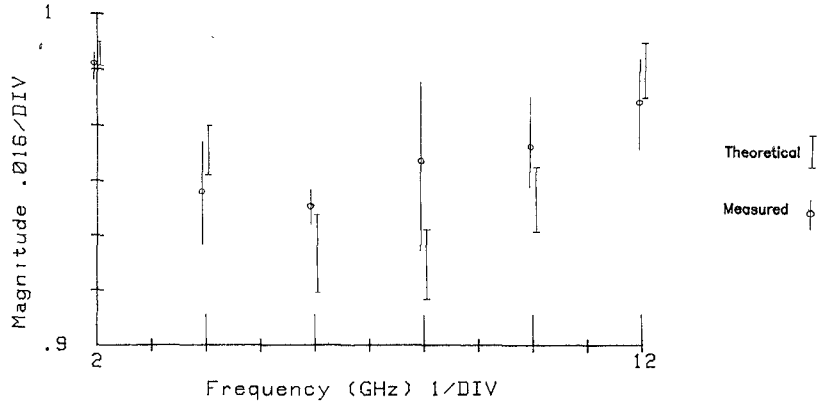

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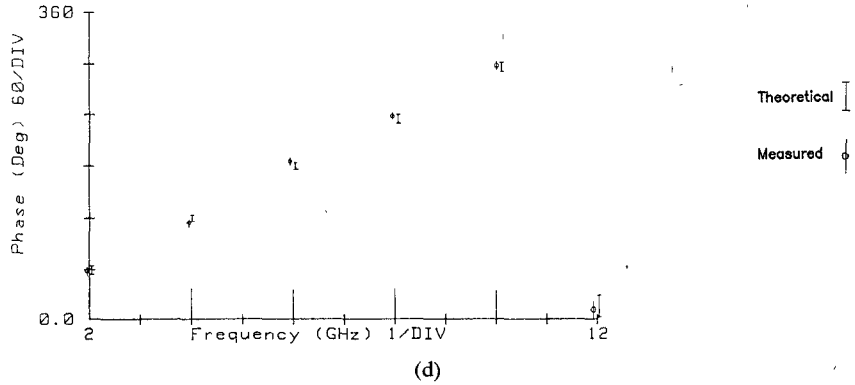


(d)

Fig. 2. Theoretical and measured S-parameters of step impedance line on alumina. (a) S_{11} magnitude. (b) S_{11} phase. (c) S_{21} magnitude. (d) S_{21} phase.

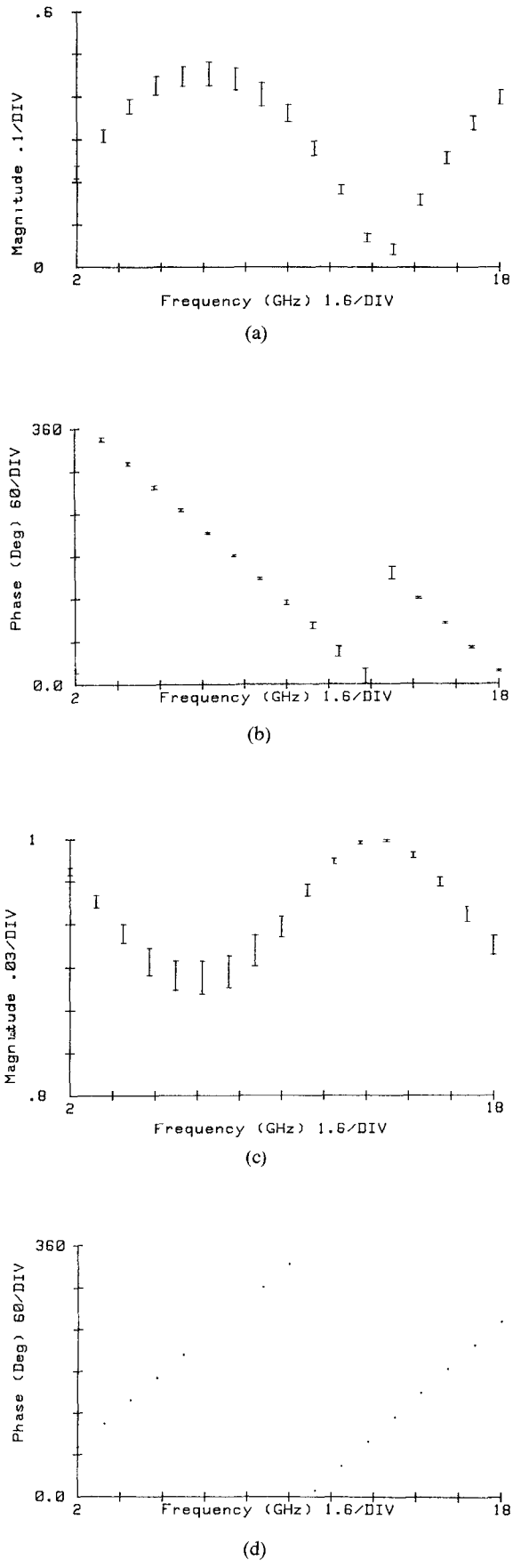


Fig. 3. Theoretical S-parameters of step impedance line on GaAs. (a) and (b) GaAs step S_{11}. (c) and (d) GaAs step S_{21}.

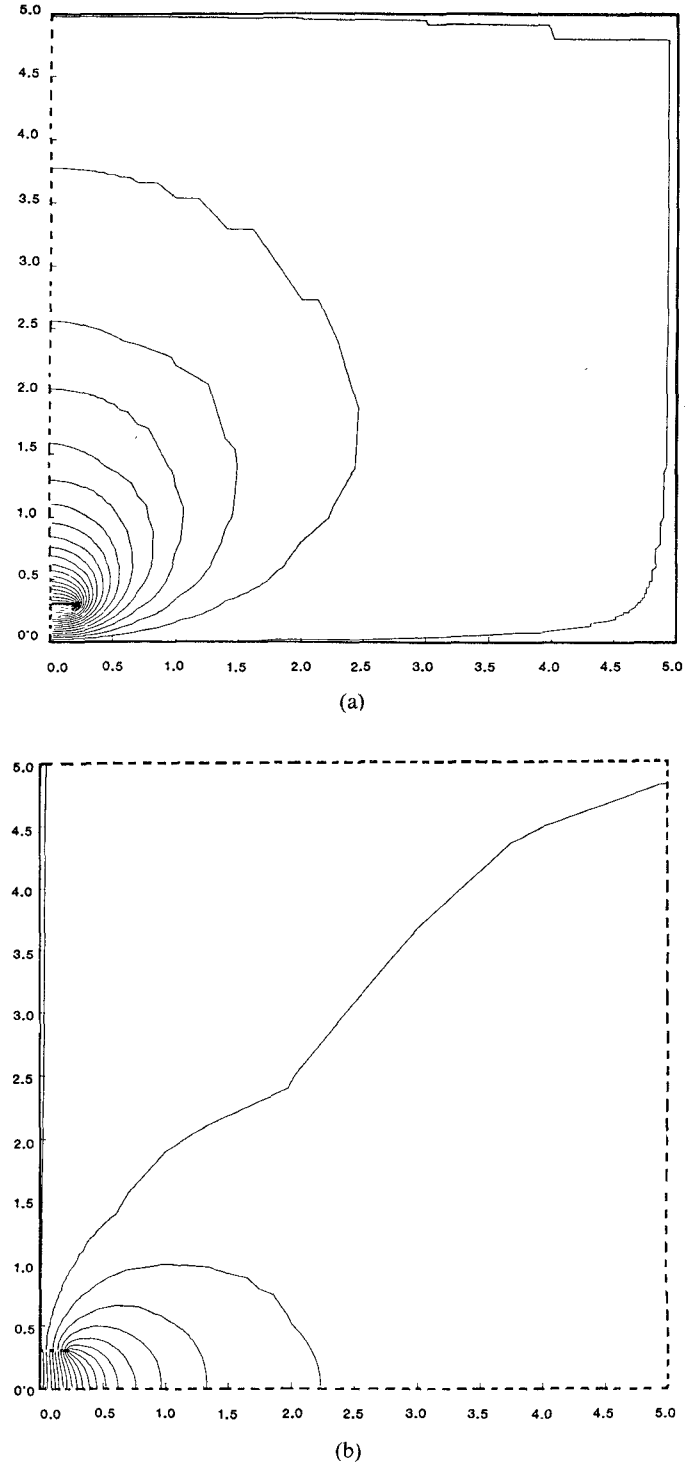
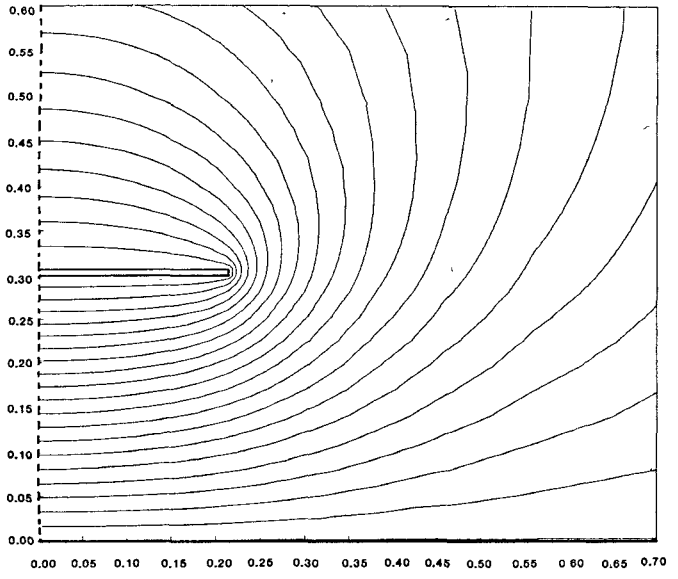
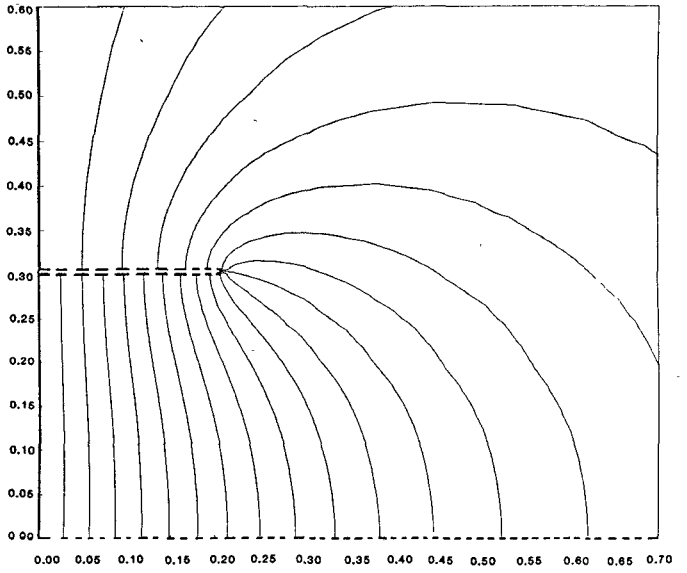


Fig. 4. Equipotential and electric-field contour plots in microstrip (1/2 section) with outer dimensions 5×5, containing dielectric with relative permittivity = 1.0.

ture and its orthogonal dual (electric field). The first contour plots in Fig. 4 refer to a microstrip structure (drawn to scale) with dielectric permittivity under the central conductor equal to unity. The contours close to the central conductor are shown in Fig. 5 with the aid of a "zoom" facility in the post-processing and clearly indicate areas of rapid field change. Figs. 6 and 7 are complementary to

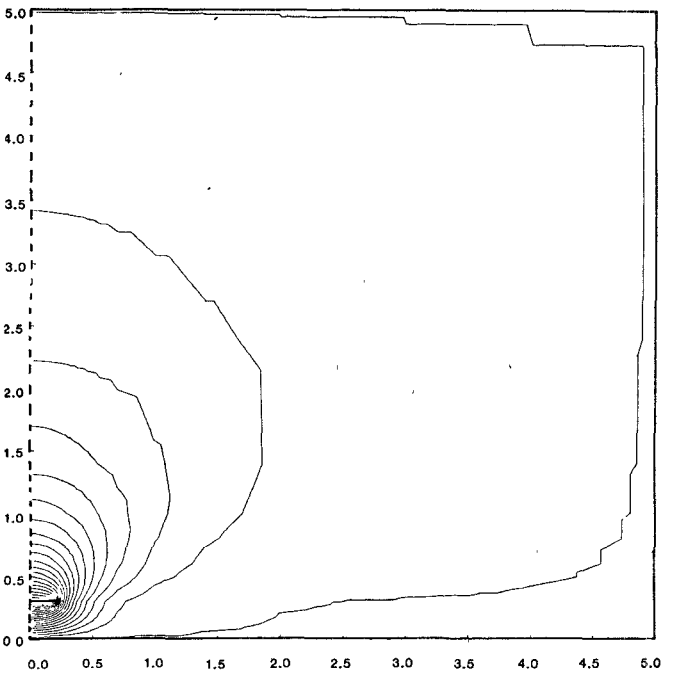


(a)

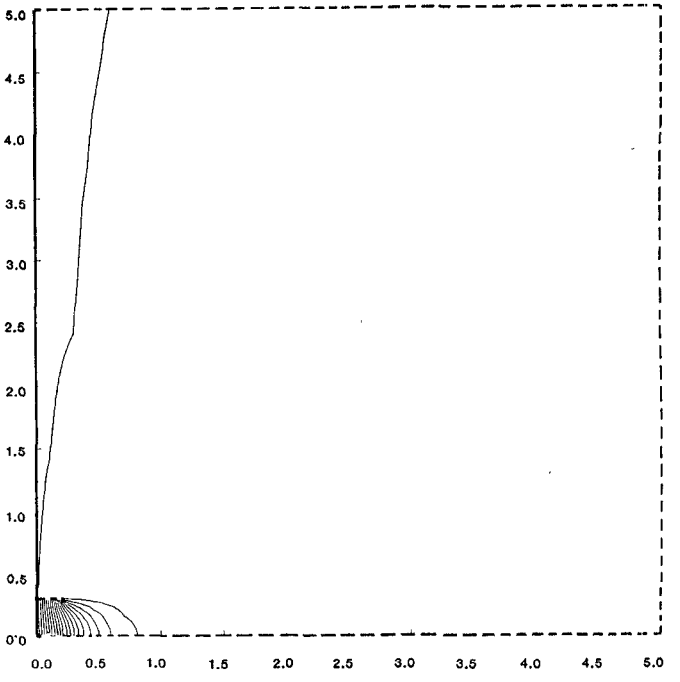


(b)

Fig. 5. Blowup of contours in Fig. 4 using the zoom post-processing facility — area surrounding the central conductor.



(a)



(b)

Fig. 6. Equipotential and electric-field contour plots in microstrip (1/2 section) with outer dimensions 5×5, containing dielectric with relative permittivity = 12.9 (GaAs substrate) under the central conductor.

Figs. 4 and 5, the only difference being the value of the dielectric permittivity (12.9 for GaAs) of the substrate underneath the central conductor.

Each of these plots is produced from processing output data from the solution to the matrix equation of order 1000 and matrix bandwidth of order 30, requiring a cpu time of 8 s and producing bounds whose difference represents a maximum error of around 2 percent.

V. Summary

In summary, both theoretical and experimental results have been presented for a microstrip test structure. New approaches have been adopted for both modeling and measurement in an attempt to independently improve the accuracy of both techniques, and so improve the confidence and reliability of design in a vital area of microwave integrated-circuit production.

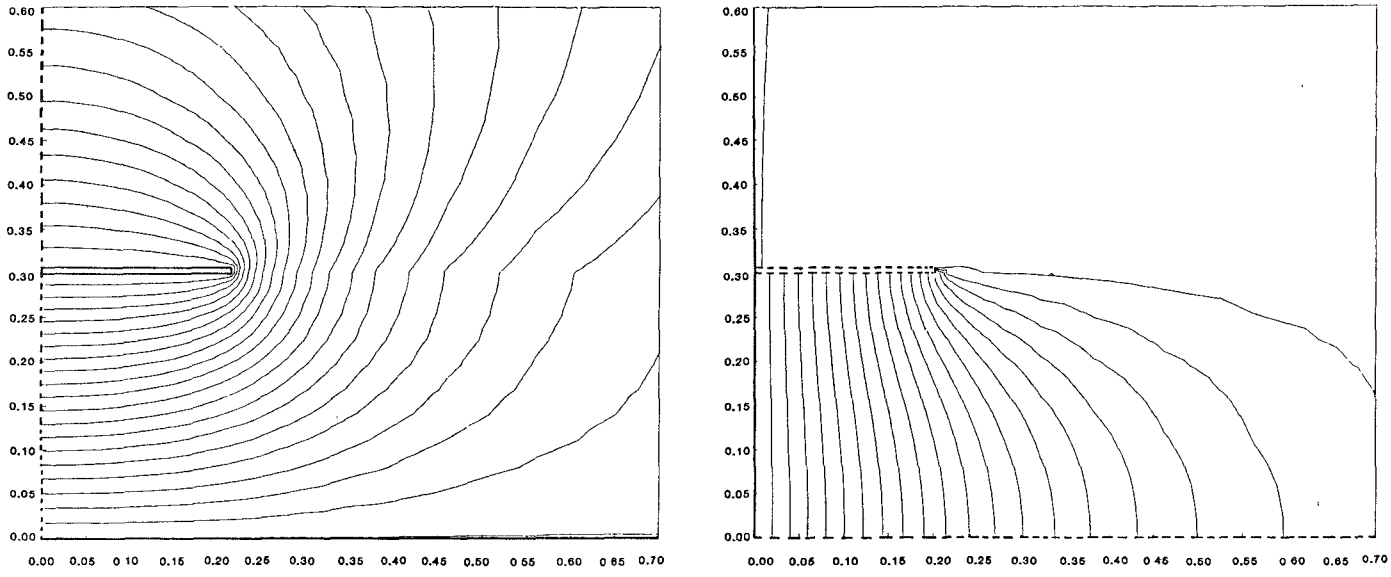


Fig. 7. Blowup of contours in Fig. 6 using the zoom post-processing facility (GaAs substrate) — area surrounding the central conductor.

REFERENCES

[1] T. C. Edwards, *Foundations of Microstrip Circuit Design*. New York: Wiley, 1981.

[2] P. Silvester, "High-order polynomial triangular finite elements for potential problems," *Int. J. Eng. Sci.*, vol. 7, p. 857, 1969.

[3] C. T. Carson and G. K. Gambrell, "Upper and lower bounds on the characteristic impedance of TEM mode transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-14, pp. 497–49, 1966.

[4] J. Fitzpatrick, "Error models for systems measurement," *Microwave J.*, pp. 63–66, May 1978.

[5] E. W. Strid and K. R. Gleason, "A dc - 12-GHz monolithic GaAs FET distributed amplifier," *IEEE Trans. Electron Devices*, vol. ED-29, July 1982.

[6] P. Daly, "Upper and lower bounds to the characteristic impedance of transmission lines using the finite element method," *Int. J. Comp. Math. In Elec. Electron. Eng.*, (COMPEL), vol. 3, no. 2, pp. 65–78, 1984.

[7] P. Daly, "Dual potential problems in transmission lines with limited or no symmetry," *Proc. Inst. Elec. Eng., Part H, Microwaves, Antennas & Propagation*, (to be published).

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P. R. Shepherd (M'83) photograph and biography unavailable at the time of publication.

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